Results for "((((data<or>clock)<near/3>recovery)<and>serdes)<in>metadata)" e-mail
Your search matched **14** of **1360403** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

((((data<or>clock)<near/3>recovery)<and>serdes)<in>metadata) Search

☐ Check to search only within this results set

Display Format: ◉ Citation ○ Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

☐ **1. A 40-43-Gb/s clock and data recovery IC with integrated SFI-5 1:16 demul technology**
Ong, A.; Benyamin, S.; Cancio, J.; Condito, V.; Labrie, T.; Qinghung Lee; Matti D.K.; Shahani, A.; Xiaomin Si; Hai Tao; Tarsia, M.; Wong, W.; Min Xu;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 12, Dec 2003 Page(s):2155 - 2168
Digital Object Identifier 10.1109/JSSC.2003.818565
AbstractPlus | Full Text: PDF(1583 KB) **IEEE JNL**
Rights and Permissions

☐ **2. Equalization and clock recovery for a 2.5-10-Gb/s 2-PAM/4-PAM backplan cell**
Zerbe, J.L.; Werner, C.W.; Stojanovic, V.; Chen, F.; Wei, J.; Tsang, G.; Kim, D W.F.; Ho, A.; Thrush, T.P.; Kollipara, R.T.; Horowitz, M.A.; Donnelly, K.S.;
Solid-State Circuits, IEEE Journal of
Volume 38, Issue 12, Dec 2003 Page(s):2121 - 2130
Digital Object Identifier 10.1109/JSSC.2003.818572
AbstractPlus | Full Text: PDF(2168 KB) **IEEE JNL**
Rights and Permissions

☐ **3. A 10-GB/s SONET-compliant CMOS transceiver with low crosstalk and in**
Werker, H.; Mechnig, S.; Holuigue, C.; Ebner, C.; Mitteregger, G.; Romani, E.; T.; Moyal, M.; Vena, M.; Melodia, A.; Fisher, J.; de Mercey, G.L.G.; Geib, H.;
Solid-State Circuits, IEEE Journal of
Volume 39, Issue 12, Dec. 2004 Page(s):2349 - 2358
Digital Object Identifier 10.1109/JSSC.2004.835652
AbstractPlus | References | Full Text: PDF(1536 KB) **IEEE JNL**
Rights and Permissions

☒ **4. Clock and data recovery with adaptive loop gain for spread spectrum Ser**
Ming-ta Hsieh; Sobelman, G.E.;
Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on
23-26 May 2005 Page(s):4883 - 4886 Vol. 5
Digital Object Identifier 10.1109/ISCAS.2005.1465727
AbstractPlus | Full Text: PDF(296 KB) **IEEE CNF**
Rights and Permissions

☒ **5. A low jitter, low power, CMOS 1.25-3.125Gbps transceiver**

Younis, A.; Boecker, C.; Hossain, K.; Abughazaleh, F.; Das, B.; Yiqin Chen; R
S.; Grung, B.;
Solid-State Circuits Conference, 2001. ESSCIRC 2001. Proceedings of the 27
18-20 Sept. 2001 Page(s):121 - 124

AbstractPlus | Full Text: PDF(1016 KB) IEEE CNF
Rights and Permissions

6. **A 10Gb/s/ch 50mW 120/spl times/130/spl mu/m/sup 2/ clock and data rec**
Kaeriyama, S.; Mizuno, M.;
Solid-State Circuits Conference, 2003. Digest of Technical Papers. ISSCC. 20
International
2003 Page(s):70 - 478 vol.1
Digital Object Identifier 10.1109/ISSCC.2003.1234211

AbstractPlus | Full Text: PDF(556 KB) | Multimedia IEEE CNF
Rights and Permissions

7. **Architecture and methodology of a SoPC with 3.25Gbps CDR based SERI dynamic phase alignment**
Venkata, R.; Wong, W.; Tran, T.; Chan, V.; Hoang, T.; Lui, H.; Ton, B.; Shumu
Lee; Shoujun Wang; Huy Ngo; Kabani, M.; Maruri, V.; Tin Lai; Tam Nguyen; Z
Luo; Toan Nguyen; Asaduzzaman, K.; Maangat, S.; Lam, J.; Patel, R.;
Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003
21-24 Sept. 2003 Page(s):659 - 662
Digital Object Identifier 10.1109/CICC.2003.1249481

AbstractPlus | Full Text: PDF(398 KB) IEEE CNF
Rights and Permissions

8. **A 62.5 Gb/s multi-standard SerDes IC**
Partovi, H.; Evans, B.; Wilson, T.; Shelton, S.; Naviasky, E.; Sanjeevi, E.; Wen
Gopalakrishnan, K.; Chokkalingam, S.; Thompson, H.; Casas, M.; Lingting Ye;
Yujing Qiu; Williams, M.; James, J.; Baldiserotto, A.; White, S.; Williams, S.; G
Gray, T.;
Custom Integrated Circuits Conference, 2003. Proceedings of the IEEE 2003
21-24 Sept. 2003 Page(s):585 - 588
Digital Object Identifier 10.1109/CICC.2003.1249466

AbstractPlus | Full Text: PDF(358 KB) IEEE CNF
Rights and Permissions

9. **A UTMI-compatible physical-layer USB2.0 transceiver chip**
Nam, J.-J.; Kim, Y.-J.; Choi, K.-H.; Park, H.-J.;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip]
17-20 Sept. 2003 Page(s):309 - 312
Digital Object Identifier 10.1109/SOC.2003.1241532

AbstractPlus | Full Text: PDF(414 KB) IEEE CNF
Rights and Permissions

10. **A compact phase interpolator for 3.125G Serdes application**
Yueming Jiang; Piovaccari, A.;
Mixed-Signal Design, 2003. Southwest Symposium on
23-25 Feb. 2003 Page(s):249 - 252
Digital Object Identifier 10.1109/SSMSD.2003.1190436

AbstractPlus | Full Text: PDF(311 KB) IEEE CNF
Rights and Permissions

11. **Effects of amplitude modulation in jitter tolerance measurements of com devices**
Ishida, M.; Yamaguchi, T.J.; Soma, M.; Musha, H.;
Test Symposium, 2002. (ATS '02). Proceedings of the 11th Asian
18-20 Nov. 2002 Page(s):45 - 48
Digital Object Identifier 10.1109/ATS.2002.1181683

AbstractPlus | Full Text: PDF(410 KB) **IEEE CNF**
Rights and Permissions

☐ **12. 1.5 Gbps, 5150 ppm spread spectrum SerDes PHY with a 0.3 mW, 1.5 Gb for serial ATA**
Sugawara, M.; Ishibashi, T.; Ogasawara, K.; Aoyama, M.; Zwerg, M.; Glowinsk Y.; Yanagita, T.; Fukaishi, M.; Shimoyama, S.; Noma, T.;
VLSI Circuits Digest of Technical Papers, 2002. Symposium on
13-15 June 2002 Page(s):60 - 63
Digital Object Identifier 10.1109/VLSIC.2002.1015045
AbstractPlus | Full Text: PDF(430 KB) **IEEE CNF**
Rights and Permissions

☐ **13. Clock and data recovery circuit for 2.5Gbps Gigabit Ethernet transceiver**
Shuguiang Li; Junyan Ren; Lianxing Yang; Fan Ye; Zhang, Y.M.M.;
ASIC, 2001. Proceedings. 4th International Conference on
23-25 Oct. 2001 Page(s):330 - 332
Digital Object Identifier 10.1109/ICASIC.2001.982567
AbstractPlus | Full Text: PDF(225 KB) **IEEE CNF**
Rights and Permissions

☐ **14. Digital serial communication device testing and its implications on auton equipment architecture**
Cai, Y.; Warwick, T.P.; Rane, S.G.; Masserrat, E.;
Test Conference, 2000. Proceedings. International
3-5 Oct. 2000 Page(s):600 - 609
Digital Object Identifier 10.1109/TEST.2000.894254
AbstractPlus | Full Text: PDF(856 KB) **IEEE CNF**
Rights and Permissions

Indexed by Inspec®

Results for "((((data<or>clock)<near/3>recovery)<and>(pattern<near/2>generator))<in>..." e-mail
Your search matched **2** of **1360403** documents.
A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

View Session History

New Search

Modify Search

((((data<or>clock)<near/3>recovery)<and>(pattern<near/2>generator))<in>metadata) Search

☐ Check to search only within this results set

Display Format: ◉ Citation ○ Citation & Abstract

» Key

IEEE JNL	IEEE Journal or Magazine
IEE JNL	IEE Journal or Magazine
IEEE CNF	IEEE Conference Proceeding
IEE CNF	IEE Conference Proceeding
IEEE STD	IEEE Standard

view selected items Select All Deselect All

☐ 1. **Design and performance of clock recovery GaAs ICs for high-speed optic communication systems**
Imai, Y.; Sano, E.; Nakamura, M.; Ishihara, N.; Kikuchi, H.; Ono, T.;
Microwave Theory and Techniques, IEEE Transactions on
Volume 41, Issue 5, May 1993 Page(s):745 - 751
Digital Object Identifier 10.1109/22.234506
AbstractPlus | Full Text: PDF(524 KB) **IEEE JNL**
Rights and Permissions

☐ 2. **A UTMI-compatible physical-layer USB2.0 transceiver chip**
Nam, J.-J.; Kim, Y.-J.; Choi, K.-H.; Park, H.-J.;
SOC Conference, 2003. Proceedings. IEEE International [Systems-on-Chip]
17-20 Sept. 2003 Page(s):309 - 312
Digital Object Identifier 10.1109/SOC.2003.1241532
AbstractPlus | Full Text: PDF(414 KB) **IEEE CNF**
Rights and Permissions